REMARKS

Claims 1-35 are pending. Claim 31 was amended to address the objection formalities. For at least the reasons set forth below, withdrawal of all outstanding rejections is respectfully requested.

Information Disclosure Statement

An Information Disclosure Statement is submitted for formal consideration of the Maloney et al. reference.

Drawings

Figs. 1A and 1B were amended to specifically label the elements for clarity. Figs. 2 and 3 were amended to make the text and references legible.

Fig. 4 was amended to show examples of semiconductor devices described in the specification.

Figs. 5 and 6 are new drawings and are added to provide detailed illustrations of Figs. 2 and 3, respectively, according to preferred embodiments of the present invention.

No new matter was entered. Each drawing amendment and the entire contents of new Figs. 5 and 6 are explicitly described in the originally filed patent application (which includes the originally filed specification and claims).

Claim Objections

Claim 31 was amended to address the claim objection informalities. Specifically, claim 31 was amended to recite that "at least two ESD-scale pulses are generated" and to provide a proper antecedent basis for the "multi-terminal semiconductor device."

Prior Art Rejections

Claims 1-6, 10, 12-15, 17-23, 28-29, 31, 32 and 35 were rejected under 35 U.S.C. 102(b) as allegedly being anticipated by Chen et al., hereafter, "Chen."

Claims 9, 26, 27, and 33 were rejected under 35 U.S.C. § 103(a), as allegedly being unpatentable over Chen.

Claims 7, 8, 24, and 25 were rejected under 35 U.S.C. § 103(a), as allegedly being unpatentable over Chen et al. in view of Kerr et al.

Claims 11, 16, and 30 were rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Chen et al. in view of Consiglio.

Claim 34 was rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Chen et al. in view of Barth et al.

Applicants respectfully traverse all of the above rejections.

1. Patentability of Independent Claims 1, 12, 18 and 31 over Chen

The Examiner asserts that all elements of independent claims 1, 12, 18 and 31 are disclosed in Chen. The applicants reviewed the reference and respectfully disagree with the Examiner's assessment.

Specifically, the Examiner asserts that Figs. 13 and 14 on page 197 of Chen shows "a biasing source generating a pulse into the gate" and that this feature is equivalent to the claimed "at least a third point of the semiconductor device receiving a second ESD-scale pulse from a second pulse generator." This is not correct. In Chen, the biasing source connected to the gate does not generate ESD-scale pulses. See page 197, column 1; line 8 through column 2 line 5 of Chen, which is repeated below for convenience.

> In a 0.18-μm salicided CMOS process, the TLP measured – characteristics of gate-driven nMOS (W/L = 300μm/0.3 μm) with 0, 0.1, and 1.1-V gate biases are shown in Fig. 13. From the experimental results in Fig. 13, the turn-on resistance is decreased from 3.8 to 2.86 when the gate bias is changed from 0 to 0.1 V. But the turn-on resistance is increased from 2.86 to 3.26 when the gate bias is increased from 0.1 to 1.1 V. In the 0.18-μm salicided CMOS process, the dependences of second breakdown currents on the gate biases of nMOS with different

> channel widths are shown in Fig. 14. The second breakdown current of nMOS with W = 300μm is initially increased from 0.69 to 1.03 A while the gate bias increases from 0 to 0.3 V. But the I_{t2} is suddenly decreased in Fig. 14 while the gate bias is only greater than 0.2 V (0.3 V) for nMOS with 100-μm (600-μm) channel width. Because only a very small voltage on the gate of the nMOS can degrade the ESD robustness of the nMOS, the gate-driven technique is hardly designed for ESD protection in the 0.18-μm salicided CMOS process. (underlining for emphasis)

As shown by this text excerpt, the biasing source voltage levels are orders of magnitude lower than typical ESD-scale levels. An example of an ESD-scale typical for semiconductor devices is taught by Chen on page 195, column 2, lines 5-8, which is repeated below for convenience.

> The average ESD level of the silicided nMOS with a channel width of 200 μm is only 0.57 kV, but that of the silicide-blocking nMOS with the same device dimension and layout style is 3 kV. (underlining for emphasis)

The biasing source referred to by the Examiner has nothing whatsoever to do with generating ESD-scale pulses.

Claims 1, 12, 18 and 31 each recite at least the following limitations that are not disclosed or suggested by Chen (underlining added for emphasis):

> at least a third point of the semiconductor device receiving a second ESD-scale pulse from the at least one pulse generator (claim 1)
>
> a second pulse generator providing a second ESD-scale pulse;...
> a third terminal of the multi-terminal device coupled to the second pulse generator to receive the second ESD-scale pulse (claim 12)
>
> providing a second ESD-scale signal to at least the third point on the semiconductor device (claim 18)
>
> providing a second ESD-scale pulse of the at least two ESD-scale pulses to at least the second terminal and a third terminal of the multi-terminal device;
> collecting ESD characteristics of the multi-terminal device under the first and second ESD-scale pulses (claim 31)

Accordingly, each of the independent claims are believed to be patentable over Chen.

2. Patentability of dependent claims

The dependent claims are believed to be patentable over the applied references for at least the reason that they are dependent upon allowable base claims and because they recite additional patentable elements and steps.

Nor do Ker, Consiglio or Berth make up for the deficiencies highlighted in Chen above.

Conclusion

Insofar as the Examiner's rejections were fully addressed, the present application is in condition for allowance. Issuance of a Notice of Allowability of all pending claims is therefore requested.

Respectfully submitted,

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Enclosure

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Amendments to the Drawings:

The attached formal drawing sheets replace the original set of formal drawing sheets.

Fig. 1A: Block 12 was labeled as "PAD."

Block 14 was labeled as "ESD Detection Circuit"

Block 18 was labeled as "Internal Circuits of an Integrated Circuit"

Fig. 1B: Block 22 was labeled to read "PAD"

Block 24 was labeled to read "ESD Detection Circuit"

Block 28 was labeled to read "Internal Circuits of an Integrated Circuit"

A label, "V_{ss}" was added to the bottom horizontal line.

Fig. 2: Block 60 was relabeled to read "Semiconductor Device (e.g., MOS, SCR, LVTSCR, FOD and BJT)"

Fig. 3: Block 60 was relabeled to read "Semiconductor Device (e.g., MOS, SCR, LVTSCR, FOD and BJT)"

Block 94 was relabeled to read "Detector (e.g., electrical analyzer)"

Block 96 was relabeled to read "Data Collector (e.g., oscilloscope)"

Fig. 4: Block 100 was relabeled to read "Providing a Semiconductor Device (e.g., MOS, SCR, LVTSCR, FOD and BJT)"

Figs. 5 and 6 were added.

Attachment: Replacement Drawing Sheets (5 sheets) for Figs. 1A, 1B and 2-4.

New Drawing Sheets (2 sheets) for Figs. 5 and 6.